UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,294	02/26/2002	Takahiro Hoshide	027260-516	5340

7590 05/08/2003

Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER
LEE, PATRICK J

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,294	HOSHIDE, TAKAHIRO	
	Examiner	Art Unit	
	Patrick J. Lee	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

/

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The disclosure is objected to because of the following informalities:

In line 16 of page 18, "numeral 201" should read "numeral 202" to accurately distinguish the referred plot data.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. With respect to claim 3, it is claimed that the data regeneration and clock recovery circuit applies the DC bias to an AC component of the voltage signal from the pre amplifier. However, such is not disclosed within the specification nor illustrated in the drawings.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 & 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Casper et al 5,754,577.

With respect to claims 1 & 3, Casper et al disclose a system for the reduction of jitter in a laser due to aging and temperature fluctuations. The system consists of photodiode (PD) as a light-receiving element and RF amplifier (120) that amplifies an AC component of the signal in line (111) as described in column 7, lines 15-20. Square law-based rectifier circuit (130) produces a DC output voltage in accordance to the amplified AC component of the output from amplifier (120) (see column 7, lines 30-33). Differential integrator (160) is part of a DC bias control circuit that applies a DC bias to the laser current driver (20) based on a high, low, or DC level of the output signal from the amplifier (see column 8, lines 6-13). Laser current driver (20) serves as a data regeneration circuit to convert voltage data into a modulating, laser-extinction current.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 & 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urala 4,805,236 in view of Price 5,721,424.

With respect to claims 1 & 3, Urala teaches an optical receiving device with improved dynamic range. The device consists of photodiode (PD) as a light-receiving device, amplifier (A_1), and bias control block (31). Photodiode (PD) produces a signal with both a DC and AC component (see Urala column 2, lines 24-28), which is amplified by transimpedance amplifier (A1). The DC component of the signal has a value of I_d, which is assumed to exceed a predetermined threshold (see Urala column 3, lines 50-52). Bias control block (31) receives a signal from amplifier (A1) and supplies a biasing voltage to diode D2, which connects to the input of amplifier (A1), serving as a feedback loop. Biasing control block (31) can inherently control the bias based of a signal with a high level, a DC level, or a low level. The portion of the output signal from the amplifier (A1) that does not reach the bias control block (31) is further processed by amplifier (A2).

However, Urala does not teach the use of a data regeneration and clock recovery circuit. Such is known and taught by Price in a photodetector circuit with DC biasing circuitry for reduction of noise (see Price column 3, lines 21-25). Price teaches the use of a clock and data regenerator (72) to obtain signals from signal amplifier (66) to produce data signal (74) and clock signal (76). To do so would have been obvious in order to adjust the level of bias with the level of power of the optical pulse stream as disclosed on column 5, lines 62-67).

Allowable Subject Matter

8. Claims 2 & 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 5 is allowable over the prior art.

10. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 2 & 4-5, the teachings of Casper et al or Urala in view of Price do not teach the use of subtracting circuits and level detectors. However, such is known, but the patentable aspect of claims 2 & 4-5 is the correction circuit that weighs the third subtraction result with the characteristics of the light receiving element and amplifier and determines the difference between the crossing point and the DC level.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kogure et al 5,636,048 teach an equalizing amplifier with a preamplifier.

Yoder 5,734,300 teaches an optical receiver preamplifier.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick J. Lee whose telephone number is (703) 305-3871. The examiner can normally be reached on Monday through Friday, 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Porta can be reached on (703) 308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9558 for regular communications and (703) 306-5511 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Patrick J. Lee
Examiner
Art Unit 2878

PJL
***
May 2, 2003

DAVID PORTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800